WHAT IS CLAIMED IS:

1. A low-voltage differential signal driver having first and second output terminals, the low-voltage differential signal driver comprising:

a current sourcing circuit adapted to generate a current;

a current steering circuit coupled to receive the generated current and first and second input signals, wherein in response to the first and second input signals the current steering circuit steers the current either in a first direction to generate a positive differential voltage across the first and second output terminals or in a second direction to generate a negative differential voltage across the first and second output terminals;

a current sinking circuit coupled to the current steering circuit and adapted to receive and sink the generated current;

a voltage dividing circuit disposed between the first and second output terminals and adapted to divide the voltage generated between the first and second output terminals;

a first voltage regulating circuit coupled to the current sinking circuit and the current steering circuit; and

a second voltage regulating circuit coupled to the current sourcing circuit and the voltage dividing circuit.

2. The low-voltage differential signal driver of claim 1, wherein said first voltage regulating circuit further comprises a first differential amplifier and wherein said second voltage regulating circuit further comprises a second differential amplifier.

3. The low-voltage differential signal driver of claim 2 further comprising a replicating circuit adapted to receive a first voltage supply and deliver a reference voltage signal to the first voltage regulating circuit.

4. The low-voltage differential signal driver of claim 3 wherein said first voltage supply supplies its voltage to the second voltage regulating circuit.

5. The low-voltage differential signal driver of claim 4 wherein said replicating circuit further comprises a third voltage regulating circuit.

6. The low-voltage differential signal driver of claim 5 further comprising a first current limiting circuitry coupled to the current sourcing circuit and adapted to limit the current flow out of the first and second output terminals during a first condition.

7. The low-voltage differential signal output driver of claim 6 further comprising a second current limiting circuitry coupled to the current sinking circuit and adapted to limit the current flow into the first and second output terminals during a second condition.

8. The low-voltage differential signal driver of claim 7 further comprising a tri-stating circuit adapted to tri-state signals present on the first and second output terminals.

9. The low-voltage differential signal driver of claim 8 wherein said tri-stating circuit is further adapted to supply a signal to the voltage dividing circuit.

10. The low-voltage differential signal output driver of claim 5 wherein said current sourcing circuit includes a first MOS transistor having a gate terminal adapted to receive an output signal generated by the second differential amplifier and a current carrying terminal coupled to a first node disposed in the current steering circuit.

11. The low-voltage differential signal output driver of claim 10 wherein said current sinking circuit includes a second MOS transistor having a gate terminal adapted to receive an output signal generated by the first differential amplifier and a current carrying terminal coupled to a second node disposed in the current steering circuit.

12. The low-voltage differential signal driver of claim 11 wherein said current steering circuit includes a third, fourth, fifth and sixth MOS transistors, wherein said third MOS transistor has a gate terminal adapted to receive the first input signal, a first current carrying terminal coupled to the first node and a second current carrying terminal coupled to the first output terminal, wherein said fourth MOS transistor has a gate terminal adapted to receive the second input signal, a first current carrying terminal coupled to the first output terminal and a second current carrying terminal coupled to the second node, wherein said fifth MOS transistor has a gate terminal adapted to receive the second input signal, a first current carrying terminal coupled to the first node and a second current carrying terminal coupled to the second output terminal, and wherein said sixth MOS transistor has a gate

terminal adapted to receive the first input signal, a first current carrying terminal coupled to the second output terminal and a second current carrying terminal coupled to the second node.

13. The low-voltage differential signal driver of claim 12 wherein said voltage dividing circuit comprises a first resistor having a terminal coupled to the first output terminal and a second resistor having a terminal coupled to the second output terminal.

14. The low-voltage differential signal driver of claim 12 wherein said voltage dividing circuit further comprises a capacitor having a first terminal coupled to the second terminal of each of the first and second resistors and a second terminal that is coupled to the ground.

15. The low-voltage differential signal driver of claim 12 wherein said first differential amplifier is further coupled to the second node.

16. The low-voltage differential signal driver of claim 12 wherein said second differential amplifier is further coupled to the first node.

17. The low-voltage differential signal driver of claim 16 wherein said first reference voltage supplied by the replicating circuit includes an offset voltage representative of a voltage drop across one of the third, fourth, fifth and sixth MOS transistors.

18. The low-voltage differential signal driver of claim 17 wherein said third voltage regulating circuit further comprises a third differential amplifier.

19. The low-voltage differential signal driver of claim 18 wherein said replicating circuit further comprises a second current source, a third resistor, a seventh MOS transistor and an eight MOS transistor, wherein a first terminal of the third resistor is coupled to a second current source and to a first input terminal of the third differential amplifier, wherein a second terminal of the third resistor is coupled to a first current carrying terminal of the seventh MOS transistor having a gate terminal coupled to a second voltage supply and a second current carrying terminal coupled to a first current carrying terminal of the eight MOS transistor, wherein a second current carrying terminal of the eight MOS transistor is coupled to the ground terminal and wherein a gate terminal of the eighth MOS transistor is

coupled to an output terminal of the third differential amplifier, and wherein a second input terminal of the third differential amplifier receives the first voltage supply.

20. The low-voltage differential signal driver of claim 19 wherein each of the first and second resistors is adapted to have a resistance equal to N/2 of the resistance of a load resistor disposed between the first and second output terminals, wherein N is greater than unity.

21. The low-voltage differential signal driver of claim 20 wherein said third resistor is adapted to have a resistance equal to M/2 of the resistance of the load resistor disposed between the first and second output terminals, wherein M is greater than unity.

22. The low-voltage differential signal driver of claim 21 wherein each of said third, fourth, fifth and sixth MOS transistors have the same channel width to channel length ratio (W/L) and wherein said seventh MOS transistor has a channel width to channel length ratio that is equal to (W/L)/M.

23. The low-voltage differential signal driver of claim 22 wherein the channel width to channel length ratio of said eight MOS transistor is equal to 1/M of the channel width to channel length ratio of the second MOS transistor.

24. The low-voltage differential signal driver of claim 23 wherein a second current carrying terminal of the first MOS transistor is coupled to the second voltage supply and wherein a second current carrying terminal of the second MOS transistor is coupled to the ground.

25. The low-voltage differential signal driver of claim 23 wherein the second current carrying terminal of the first MOS transistor is coupled to a first terminal of a fourth resistor and to a gate terminal of a ninth MOS transistor having a first current carrying terminal coupled to the second voltage supply and a second current carrying terminal coupled to a first terminal of a fifth resistor and a gate terminal of a tenth MOS transistor, wherein the second terminal of the fourth resistor is coupled to the second voltage supply and wherein the second terminal of the fifth resistor is coupled to the ground terminal, wherein a first current carrying terminal of the tenth MOS transistor is coupled to the ground terminal and wherein the second current carrying terminal of the tenth MOS transistor is coupled to the gate terminal of the first MOS transistor.

26. The low-voltage differential signal driver of claim 25 wherein the second current carrying terminal of the second MOS transistor is coupled to a first terminal of a sixth resistor and to a gate terminal of an eleventh MOS transistor having a first current carrying terminal coupled to the ground and a second current carrying terminal coupled to a first terminal of a seventh resistor and a gate terminal of a twelfth MOS transistor, wherein the second terminal of the sixth resistor is coupled to the ground and wherein the second terminal of the seventh resistor is coupled to the second supply voltage, wherein a first current carrying terminal of the twelfth MOS transistor is coupled to the second voltage supply and wherein the second current carrying terminal of the twelfth MOS transistor is coupled to the gate terminal of the second MOS transistor.

27. A method for supplying a low-voltage differential signal across first and second terminals, the method comprising:

generating a current using a first voltage;

steering the generated current in a first direction to generate a positive differential output voltage across the first and second terminals in response to a first set of input signals and steering the generated current in a second direction to generate a negative differential output voltage across the first and second terminals in response to a second set of input signals;

dividing the differential output voltage generated between the first and second input terminals to generate a weighted average thereof;

regulating the weighted average of the differential output voltage;

sinking the generated current; and

regulating the first voltage.

28. The method of claim 27 wherein the weighted average of the differential output voltage is regulated using an operational amplifier that receives a first supply voltage at one of its input terminals.

29. The method of claim 28 wherein the first voltage is regulated using a reference voltage generated by a replicating circuit.

30. The method of claim 29 further comprising:

limiting the current flowing out of or into the first and second output terminals.

31. The method of claim 30 low-voltage further comprising: tri-stating the differential output voltage.